Jani Babu Shaik

Email: sb638@snu.edu.in
LinkedIn: linkedin.com/in/skjanibabu786/
Hostel-2C, Shiv Nadar University
Mobile: +91-7207224309

EDUCATION

Shiv Nadar University (accorded Institute of Eminence status by Govt. of India) Greater Noida, India
Ph.D., Microelectronics Design; CGPA: 9.56 Jan 2017 - Dec 2021

- Thesis: "Design and Analysis of Reliability-Aware CMOS Circuits for a Neuromorphic System"
- Received Shiv Nadar Foundation Scholarship

National Institute of Technology (NIT) Hamirpur, India
M. Tech., VLSI Design Automation & Techniques; CGPA: 7.97 Jul 2014 - Jul 2016

- Dissertation: *"Analysis and Implementation of Image Processing Filters on FPGA"*
- Received MHRD-India scholarship

EXPERIENCE

Doctoral Research Scholar **Shiv Nadar University**
Supervisor: *Dr. Sonal Singhal* Jan 2017 – till now
Project: "Design and Analysis of Reliability-aware CMOS circuits for a Neuromorphic System" funded by Shiv Nadar Foundation

- Investigated the impact of data-dependent BTI degradation and process variability on SRAM metrics
- Analyzed the impact of BTI and HCI on various spike-event generation neuromorphic circuits
- Proposed a low-power and reliability-aware neuromorphic circuits
- Integrated the SRAM memory block and reliable-aware neural core to design a neuromorphic system

Internship Program **Entuple Technolgies Pvt. Ltd**
Physical Design and Verification Internship Program Aug 2020 – Oct 2020

- Executed the RTL and Physical Synthesis flow of UART using Cadence Genus
- Carried out static timing analysis (STA) using the Cadence Tempus tool
- Performed physical design analysis for the I2C netlist using the Cadence Innovus tool
- Completed internship and earned STAR certificate for achieving a good grade in quizzes and assignments

Graduate Researcher **NIT Hamirpur**
Advisor: *Dr. Philemon Daniel* Jun 2015 - Jul 2016
Project: "Analysis and Implementation of Image Processing Filters on FPGA" funded by MHRD-India

- Reviewed various image processing filters using Matlab for autonomous driver assist system
- Generated HDL code for image processing filters using Matlab HDL coder and Vivado HLS tools
- Created IPs of these filters and executed them on ZYBO to analyze their performance in real-time

SKILLS

- *Operating Systems:* Windows, Linux (Ubuntu and RHEL)
- *Programming Languages:*C, C++, Python, MATLAB
- *Software Tools:* Microsoft Office Tools, Origin, MATLAB, MS visual studio code, Latex, ENDNOTE, MENDELEY desktop, *NeuroSim* simulator
- *EDA SKILLS & TOOLS*:

VLSI Circuit Simulation	**Tools:** Cadence-Virtuoso (ADE, ADEXL), Synopsys-HSPICE, LT-SPICE, Tanner SPICE
Layout Editing & Analysis	**Tools:** Cadence-Layout XL, Tanner Layout
RTL Synthesis	**Tools:** Xilinx
Physical Designing	**Tools:** Explored: Cadence Genus, Innovus, Tempus
Hardware Description Language	Verilog, basic of VHDL and SystemVerilog, Verilog-A
Hands on Electronics Hardwares	ZYBO, Nexys4 student, STM32, Arduino, Digital Oscilloscope
Device Modelling	Synopsis Sentaurus TCAD

RESEARCH PROJECT

Micro-controller based Internet of Things for agriculture sensors data on cloud Jan 2022 – Present

- Developed Arduino-based embedded system which collects the data from multiple agriculture fields and send to cordniator node through LoRa communication protocal.
- Collected sensor data sends to cloud server through MQTT protocal

Design and analysis of low-power and reliability-aware Configurable SRAM-based In-Memory Computing System Nov 2021 – Present

- Investigating various SRAM-based In-Memory computing (IMC) system available in the literature
- Developing a configurable In-memory computing architecture which includes Logic functionality and Content addressable memory (CAM)
- Proposing an energy-efficient and reliability-aware configurable SRAM-based IMC architecture

Design and analysis of reliability-aware of Integrate-and-Fire Silicon Neurons for a Neuromorphic System Jun 2018 – Feb 2022

- Investigated the impact of CMOS reliability and process variability issues on various neuromorphic circuits.
- Proposed the mitigation technique for minimizing the degradation of circuit performance after lifetime.
- Designed and proposed a reliability-aware programmable memory Neuromorphic system (rel-SLIFMEM)

Implementation of Spiking Neural Network (SNN) for Image Classification Jun 2020 – Aug 2021

- Designed and implemented a Simplified Spiking Neural Network model with an standard STDP learning algorithm for image classification
- GitHub URL: https://github.com/pranika98/SNN_minor_project

Design and analysis of memristive CROSSBAR Architecture for better read stability and write-ability Apr 2021 – Dec 2021

- Designed Memristive CROSSBAR architecture with low leakage (sneakpath) currents.
- Charcterized and propose an improvement method for increase read and write stability of CROSSBAR

Energy Efficient, reliability-aware design of Temporal Neuromorphic Encoder Feb 2020 – Dec 2021

- Investigated the impact of BTI and HCI on conventional temporal neuromorphic encoder
- Formulated a mathematical model between image pixels intensity and the inter-spike-intervals (ISIs) for image encoding
- Designed and proposed an energy-efficient and reliability-aware Temporal Neuromorphic Encoder

Impact of different NBTI induced Variability on SRAM stability for FinFET Sep 2019 – Dec 2021

- Retrived and generated NBTI variability of experimental data from different semiconductor industries
- Investigated the impact of NBTI variability on FinFET SRAM stability

Investigation of SRAM stability under the influence of data-dependent BTI degradation and process variability at HKMG Technology Feb 2017 – Dec 2019

- Comprehended various SRAM metrics obtained from distinguished measurement techniques
- Investigated the impact of data-dependent BTI degradation under continuous/non-continuous gate bias along with process variability on these SRAM metrics

JOURNAL ARTICLES

- **Jani Babu Shaik**, S. Singhal, and N. Goel, "Analysis of SRAM metrics for data dependent BTI degradation andprocess variability", Integration the VLSI Journal, 72 (2020) 148-162. DOI: 10.1016/j.vlsi.2020.01.006
- S.M. Picardo, **Jani Babu Shaik**, N. Goel, S. Singhal, "Integral Impact of PVT variation with NBTI degradation on SRAM dynamic and static performance metrics", International Journal of Electronics, 109(2), 2021. DOI: 10.1080/00207217.2021.1908628
- **Jani Babu Shaik**, Aaditiya VS, S. Singhal, N. Goel "Reliability-aware design of Neuromorphic Temporal Encoder for Image Recognition", International Journal of Circuit Theory and Applications, (2021) DOI: 10.1002/cta.3209
- **Jani Babu Shaik**, S. Singhal, S. M. Picardo, and N. Goel, "Impact of various NBTI distributions on SRAM performance for FinFET technology", Integration the VLSI Journal, (2021). DOI: 10.1016/j.vlsi.2021.12.005
- **Jani Babu Shaik**, S. M. Picardo, S. Singhal, and N. Goel, "Reliability-Aware Design of Integrate-and-Fire Silicon Neurons", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (submitted to the Journal for peer review)
- S. M. Picardo, **Jani Babu Shaik**, S. Singhal, N. Goel, "Enabling Efficient Rate and Temporal Coding using Reliability-Aware Design of a Neuromorphic Circuit", International Journal of Circuit Theory and Applications, (submitted to the Journal for peer review)
- **Jani Babu Shaik**, S.Singhal, N. Goel, "Design and Analysis of a Energy-effiecient and Reliability-Aware Simplified Neuromorphic System" Microelectronics Journal (Ready to communicate with Journal)
- Xinfei Guo, Linyu Zhu, **Jani Babu Shaik**, and Mircea R. Stan. "Extending Chip Lifetime for Sustainable and Reliable Computing: A Review" (Manuscript under Preparation)

CONFERENCE PROCEEDINGS

- **Shaik Jani Babu**, S.P. Chaudhari, S. Singhal, and N. Goel, "Analyzing Impact of NBTI and Time-Zero Variability on Dynamic SRAM Metrics", 2018 INDICON, Coimbatore, 2018
- S. P. Chaudhari, **Shaik Jani Babu**, S. Singhal, and N. Goel, "Correlation of Dynamic and Static Metrics of SRAM Cell under Time-Zero Variability and after NBTI Degradation", IEEE iSES, Hyderabad, 2018
- **Jani Babu Shaik** et al., "Investigating the impact of BTI and HCI on log-domain based Mihalas-Niebur Neuron circuit", MoSICom 2020
- P. K Gill, **Jani Babu Shaik**, S. Singhal, and N.Goel, "FPGA implementation of Random Feature Mapping in ELM algorithm for binary classification", MoSICom 2020
- S. M. Picardo, **Shaik Jani Babu**, S. Sahni, S. Singhal, N.Goel, "Analyzing the Impact of NBTI and Process Variability on Dynamic SRAM Metrics Under Temperature Variations", MoSICom 2020
- Aadithya VS, **Jani Babu Shaik**, S. Singhal, and S. M. Picardo, N. Goel, "Design and Mathematical Modelling of Inter Spike Interval of Temporal Neuromorphic Encoder for Image Recognition", IEEE 5th International Conference on Emerging Electronics (ICEE) 2020 (**in press**)
- S. M. Picardo, **Shaik Jani Babu**, S. Singhal, N.Goel, "Device Reliability Affecting Coding Schemes in Neuromorphic Circuits", in IEEE TenSymp 2022 (accepted)
- **Jani Babu Shaik**, S. M. Picardo, S. Singhal, and N. Goel, "Impact of Reliability Issues and Process Variability in Neuromorphic Circuits", IEEE TenSymp 2022 (accepted)

TEACHING EXPERIENCE

Shiv Nadar University — Greater Noida, India
Teaching Assistant — Jan 2017 – Dec 2021
Assisted faculties in laboratory research and aided students during review sessions for the following courses:

- VLSI Design and Technology (EED401)
- Analog CMOS VLSI Design (EED361)
- Digital System Design with FPGAs (EED359)
- Embedded Systems Hardware (EED308)
- Applied Machine Learning (EED363)
- Digital Electronics (EED206)
- Analog Electronics (EED204)
- Basic Electrical Engineering (EED103)

National Institute of Technology (NIT) — Hamirpur, India
Teaching Assistant — Aug 2014 – Apr 2016
Assisted faculties in the laboratory for the following courses:
Microcontroller and Embedded Systems; CAD of Integrated Circuits; Basic Electrical Engineering

PROFESSIONAL ACTIVITIES AND AFFLIATIONS

Journal Paper Reviewer

Integration-the VLSI Jornal
International Journal of Circuit Theory and Applications
Journal of Engineering Research and Sciences

Conference Paper Reviewer

Third International Conference on Computing and Network Communications (CoCoNet'19), 2019
International Conference on Modelling Simulation & Intelligent Computing, 2020
2022 IEEE International Midwest Symposium on Circuits and Systems, 2022

Membership

IEEE Student membership, 2018-present

RECENT WORKSHOPS AND CERTIFICATIONS

Short Course in Modeling and Simulation of Nano Transistors — Remote
Organized by NanoLab @ IIT Kanpur — Feb 2021 – Mar 2021

- Participated in the workshop to learn different aspects of Nano Transistors such as compact modeling, TCAD simulations, Electrical characterization
- Trained in different Electronic Design Automation (EDA) tools

Tutorial Session in Neuromorphic Devices — Remote
Organized by IIT Delhi — Nov 2020

- Participated tutorial session on the importance of neuromorphic computing in today's world and how emerging devices are part of next-generation computing.

PROFESSIONAL REFERENCES

Available on request